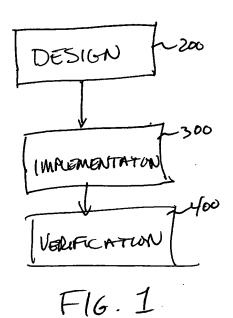
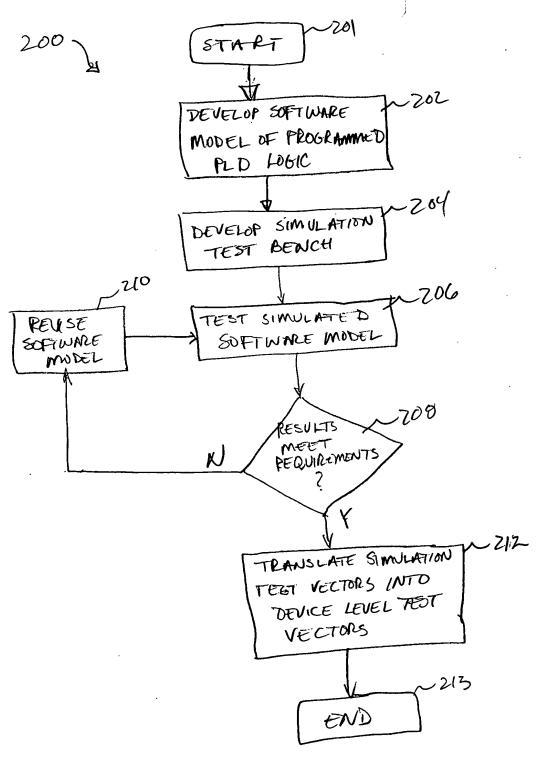
100 %





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In re: Jeff C. Klein, et al.
Serial No.: To Be Assigned
itle: Verification Test Method for Programmable Logic Devices
Docket No.: H0002065
Sheet 3 of 6

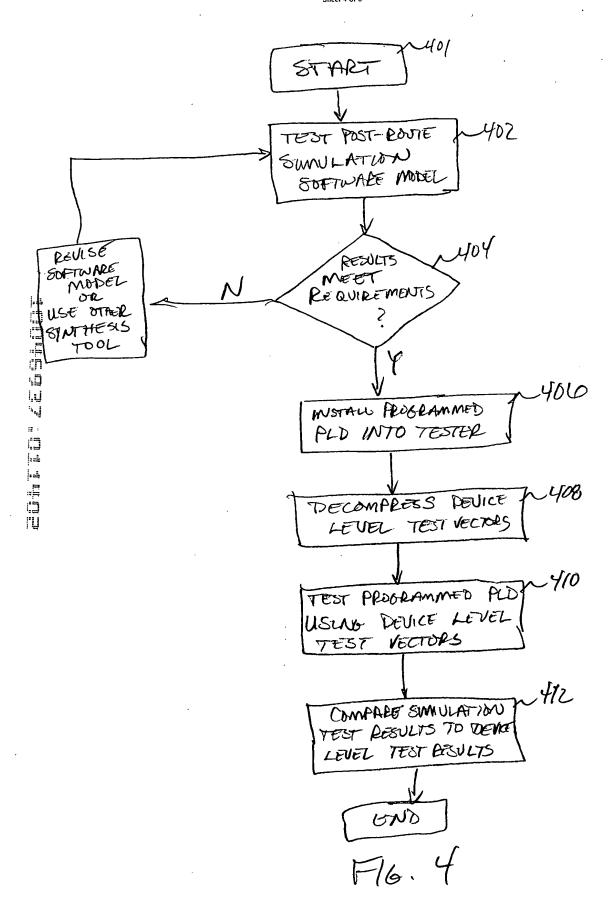
SHART
SHART
SHARTE JOSOZ
SOFTWARE
MODEL

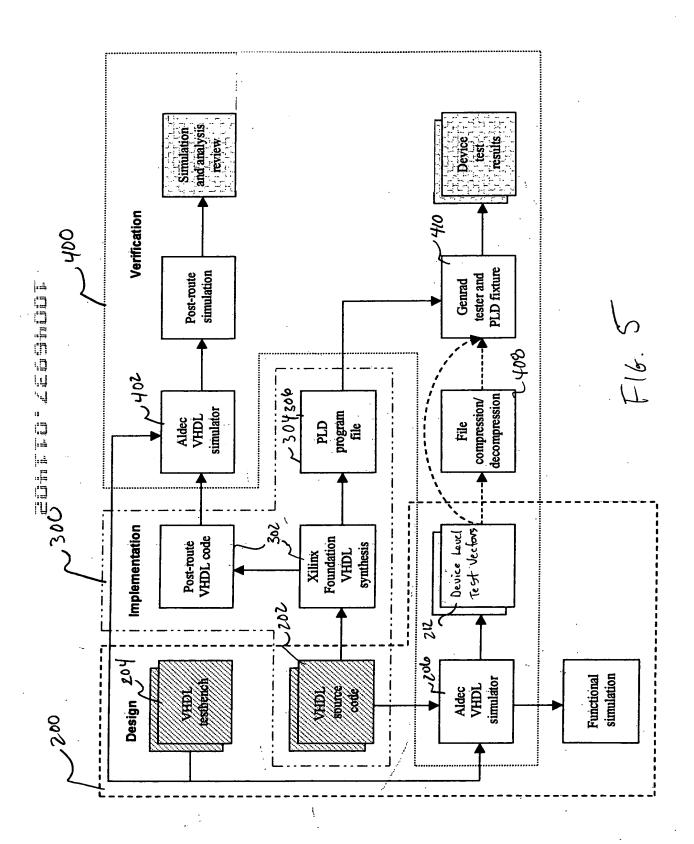
GENERATE JOSOY
PLD PROGRAM
FILE

DOWNLOAD
INTO
DEVICE

END
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F16.3





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